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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,852	03/12/2004	Isamu Miyanishi	2271/71532	2074

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EXAMINER	
ZAMAN, FAISAL M	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,852	MIYANISHI ET AL.	
	Examiner	Art Unit	
	Faisal Zaman	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The references listed on the Information Disclosure Statement submitted on 12 March 2004, have been considered by the examiner (see attached PTO-1449).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claim 19** is rejected under 35 U.S.C. 102(e) as being anticipated by Tsuda et al. ("Tsuda") (U.S. Patent No. 6,799,242).

Tsuda discloses an optical disk drive apparatus (title, abstract), comprising:

an optical disk drive mechanism (Figure 1, Column 1, lines 19-23); and

an interface circuit for interfacing communications, between the optical disk drive mechanism and a host computer (Figure 7, Column 7, lines 17-28), the interfacing circuit comprising:

an input terminal for receiving data sent from the host computer (Figure 7, item 13, Column 2 lines 35-40);

a data processor configured to perform a predetermined data processing operation to the data received through the input terminal (Figure 7, item 250, Column 7, lines 17-28);

a clock generator configured to generate a clock signal with which the data processor performs the predetermined data processing operation (Figure 7, item 62, Column 8, lines 11-25);

an operation mode changer configured to control the clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode (Column 7 line 56 – Column 8 line 10);

a buffering circuit block configured to buffer the data received through the input terminal (Figure 7, item 260, Column 7, lines 23-28), the buffering circuit block including:

a first data transfer path configured to transfer the data received through the input terminal to the data processor not via a memory (Column 7, lines 1-5), and

a second data transfer path configured to transfer the data received through the input terminal to the data processor via a memory (Column 7, lines 6-16); and

a path selection controller configured to control the buffering circuit clock to select the second data transfer path (Column 7 lines 1-16) on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode (Column 7 line 56 – Column 8 line 10).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-3, 7, 9-12, 16, and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuda in view of Matsumoto et al. ("Matsumoto") (U.S. Patent No. 6,373,598).

Regarding Claim 1, Tsuda discloses a communications interface apparatus comprising:

A register circuit storing data to be transferred to a host computer (Figure 7, item 7, Column 7 lines 62-67, "buffer RAM" in the prior art reference is considered equivalent to the "register circuit" of the current application, because both devices store data to be sent to the host computer, see Column 2 lines 35-40);

A first memory storing first information indicating a specific address of the register circuit and representing an access to the communications interface apparatus executed by the host computer for a data transfer (Figure 7, item 230, Column 7 lines 29-33, "address register" in the prior art reference is considered equivalent to the "first memory" of the current application because they both store the address of the register circuit);

A second memory storing second information, sent from the host computer in association with the first information stored in the first memory, to be written into the register circuit at the specific address indicated by the first information stored in the first memory (Column 7 line 62 – Column 8 line 4, "register of the microcomputer interface"); and

Two control circuits configured to perform an information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed (Tsuda, Figure 7, item 232, Column 7 line 62 – Column 8 line 4).

Tsuda does not, however, disclose that a single control circuit is used to perform the action in the above paragraph.

In the same field of endeavor (e.g. a communications link between one or more devices) Matsumoto teaches a control circuit configured to perform an information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed (Matsumoto, Column 12, lines 36-39, "a single control means for controlling a selected one of first storage device and said second storage device to store information").

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated Matsumoto's teachings of using a single control circuit rather than two control circuits with the teachings of Tsuda, for the purpose of effectively using a storage area of a hard disk of a personal computer to improve control efficiency (see Matsumoto, Column 2, lines 22-26). It would be obvious

to one of ordinary skill in the art to combine in order to have a single control circuit rather than two control circuits to have an efficient system while reducing power consumption for the system disclosed in Tsuda.

Regarding Claim 2, Tsuda discloses wherein the control circuits perform the information writing operation to write the first information into the first memory and the second information into the second memory in chronological order of accesses executed, when an operation mode of the communications interface apparatus is changed from a low power consumption mode to a regular operation mode (Column 8, lines 19-25, "sleep mode" in the prior art reference is considered equivalent to "low power consumption mode" in the current application).

Regarding Claim 3, Tsuda discloses wherein the control circuits perform an information reading operation for reading the first and second information written in the first and second memories, respectively, in chronological order of the accesses executed and an information transfer operation to transfer the first and second information read from the first and second memories, respectively, to the register circuit in chronological order of the accesses executed, when the operation mode of the communications interface apparatus is changed from the low power consumption mode to the regular operation mode (Column 8 lines 19-25, and Column 8 line 63 – Column 9 line 2).

Regarding Claim 7, Tsuda discloses wherein each of the first and second memories comprises a selection circuit (Figure 6, Column 7, lines 1-16) configured to select one of (i) a first data path for the first and second information not via the first and second memories (Column 7, lines 1-5) and (ii) a second data path for the first and second information via the respective first and second memories, on-an exclusive basis according to a control signal from the control circuit and to output corresponding data to the register circuit through the selected one of the first and second data paths (Figure 6, Column 7, lines 6-16, although the prior art reference does not specifically mention the second data path in the text, it would be obvious to one of ordinary skill in the art to see in Figure 6 that the switch could be connected to the second data path also shown in the figure).

Regarding Claim 9, Tsuda discloses wherein the register circuit, the first and second memories, and the control circuit are integrated into a single integrated chip (Column 9, lines 47-50).

Regarding Claim 10, all the same elements of Claim 1 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 1 applies equally as well to Claim 10.

Regarding Claim 11, all the same elements of Claim 2 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 2 applies equally as well to Claim 11.

Regarding Claim 12, all the same elements of Claim 3 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 3 applies equally as well to Claim 12.

Regarding Claim 16, all the same elements of Claim 7 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 7 applies equally as well to Claim 16.

Regarding Claim 18, all the same elements of Claim 9 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 9 applies equally as well to Claim 18.

Claim Rejections - 35 USC § 103

6. **Claims 4-6, 8, 13-15, and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuda, in view of Matsumoto, further in view of Yamada et al. ("Yamada") (U.S. Patent No. 6,470,439).

Tsuda discloses the invention substantially as claimed.

Regarding Claim 4, Tsuda discloses wherein the control circuits conduct the information writing operations with respect to the first and second memories in synchronism with each other and conducts the information reading operations with respect to the first and second memories in synchronism with each other (Tsuda, Column 7 line 62 – Column 8 line 10, the prior art reference describes how the read and write procedure continues on until all the data has been transferred).

In same field of endeavor (e.g. the use of a memory control circuit in controlling FIFO memory used in various electronic devices), Yamada teaches the following limitation, which Tsuda does not expressly disclose:

Wherein each of the first and second memories comprises a first-in and first-out memory including a specific number of buffer areas into which data from the host computer is written (Yamada, Column 3, lines 18-25).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have incorporated Yamada's teachings of the use of a memory control circuit in controlling FIFO memory used in various electronic devices with the teachings of Tsuda and Matsumoto, for the purpose of providing a FIFO memory control circuit in which the amount of effective data in a memory can be correctly counted so that when the frequencies of a read clock and a write clock are different, data is prevented from being lost by being overwritten, and data is prevented from being read out twice (see Yamada, Column 6 lines 18-22). Tsuda provides motivation to combine by stating it is an object of the present invention to have an

efficient system while reducing power consumption in a device during a sleep mode (see Tsuda, Column 3, lines 28-30).

Regarding Claim 5, Yamada discloses the following, which Tsuda or Matsumoto do not disclose expressly:

Wherein the control circuit accesses the first and second memories in synchronism with a first clock signal for the information writing operation and a second clock signal for the information reading operation (Yamada, Column 3, lines 26-31), and wherein a first frequency of the first clock signal is greater than a second frequency of the second clock signal (Yamada, Column 4, lines 43-52).

The motivation that was utilized in the combination of Claim 4, super, applies equally as well to Claim 5.

Regarding Claim 6, Tsuda discloses wherein the control circuit transfers the first and second information directly to the register circuit, without buffering the first and second information in the first-in and first-out memories of the first and second memories (Tsuda, Column 7 lines 1-5, it would be obvious to one of ordinary skill in the art to combine this reference with Tsuda, Column 8, lines 19-24 in order to have data sent directly to the register circuit when power is changed from low to regular operation mode).

Yamada discloses the following limitation, which Tsuda does not disclose expressly: in an event that the respective first-in and first-out memories of the first and

second information stored in the respective first-in and first-out memories of the first and second memories, respectively, are transferred to the register circuit (Yamada, Column 4, lines 12-22) when the operation mode of the communications interface apparatus is changed from the low power consumption mode to the regular operation mode (disclosed in Tsuda, see previous paragraph).

The motivation that was utilized in the combination of Claim 4, super, applies equally as well to Claim 6.

Regarding Claim 8, Tsuda discloses wherein the control circuits comprise:

a data writing circuit block configured to write the first and second information into the first and second memories, respectively, in accordance with an access performed by the host computer (Tsuda, Figure 7, item 232, Column 7 line 62 – Column 8 line 4);

a data reading circuit block configured to start reading the first and second information from the first and second memories, respectively, upon a time the write control circuit block starts writing the first and second information into the first and second memories, respectively (Tsuda, Figure 7, item 232, Column 7 line 62 – Column 8 line 4);

a selection control circuit block configured to control the selection circuits included in the respective first and second memories in accordance with a status as to whether the operation mode of the communications interface apparatus is the low power consumption mode (Tsuda, Column 7 line 57 – Column 8 line 10) and the status

signal output from the status detecting circuit block (disclosed in Yamada, see next paragraph).

Yamada discloses the following, which Tsuda does not disclose expressly: a status detecting circuit block configured to detect memory statuses of the first-in and first-out memories included in the respective first and second memories and to output a status signal representing the memory statuses detected (Yamada, Column 4, lines 12-28).

The motivation that was utilized in the combination of Claim 4, super, applies equally as well to Claim 8.

Regarding Claim 13, all the same elements of Claim 4 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 4 applies equally as well to Claim 13.

Regarding Claim 14, all the same elements of Claim 5 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 5 applies equally as well to Claim 14.

Regarding Claim 15, all the same elements of Claim 6 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 6 applies equally as well to Claim 15.

Regarding Claim 17, all the same elements of Claim 8 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 8 applies equally as well to Claim 17.

Prior Art of Record

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lewis et al. (U.S. Patent No. 5,701,417) discloses a method and apparatus for providing initial instructions through a communications interface in a multiple computer system. Mendenhall et al. (U.S. Patent No. 6,341,198) discloses a system for byte packing multiple data channels in an MPEG/DVD system. Van Cruyningen (U.S. Patent No. 6,338,110) discloses partitioning of storage channels using programmable switches. Johnson et al. (U.S. Patent No. 5,832,262) discloses a realtime hardware scheduler utilizing processor message passing and queue management cells. Ober (U.S. Patent No. 6,665,802) discloses a power management and control system for microcontroller. Velasco et al. (U.S. Patent No. 6,813,674) discloses a dual-edge FIFO interface. Chu et al. (U.S. Patent Publication No. 2004/0015731) discloses intelligent management of a hard disk drive. Mitchell et al. (U.S. Patent No. 5,987,614) discloses a distributed power management system and method for a computer. Walter et al. (U.S. Patent No. 4,980,857) discloses an operations controller for a fault tolerant multiple node processing system. Hussein (U.S. Patent No. 6,285,521) discloses a disk drive employing power source modulation for reducing power consumption.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6459. The examiner can normally be reached on Monday thru Friday, 9 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

fmz

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SUPERVISORY PATENT EXAMINER
10/24/05